

ZSP® Audio & Video Application Software



As product and design complexity continue to escalate, so has software complexity. Often when faced with the high costs to manufacture an IC, software development costs are sometimes easy to miss. However, when evaluating a processor for your next product line, it is essential that these software development costs are also considered.

According to International Business Strategies (IBS), SoC embedded software development effort has grown by more than 400% over the last few years. 90 nm SoCs will push the cost of software development past the 56% of the total SoC design effort it now comprises.

Several factors dramatically influence software development costs: ease of programming, scalability in processor product line, availability of third party developers familiar with the architecture and finally, availability of existing modules.

VeriSilicon's comprehensive software development tools offer a cost effective solution, with the added benefits of ease, scalability and a community of experienced third party developers to meet your software development needs.

Processor Scalability



As often is the case, evolving product needs may overload the capabilities of a part in production. Ability to address the increased performance requirements in a new SoC from the same processor vendor may be difficult if software compatibility is not supported in their products. In these cases, existing software modules may have to be totally rewritten, resulting in high development costs and a potential loss of time-to-market.

This is not the case with the VeriSilicon ZSP family of cores. Within a ZSP generation family, all cores are binary software compatible, and across ZSP generation families, cores are assembly-level software compatible. As a result, ZSP processors enable an easy and quick migration path for system developers.

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Comprehensive Set of ZSP Software

Since the ZSP400's introduction in 1998, numerous DSP software modules have been ported and optimized to the ZSP Architecture. The complete set of ZSP software has outpaced other DSP processor vendors and continues to gain traction with the rapid rate of ZSP software development. The availability of these optimized, pre-verified software libraries reduces both customers' development time and cost.

Optimized SW for

- ZSPneo
- ZSP200
- ZSP210
- ZSP400
- ZSP410
- ZSP500
- ZSP510
- ZSP520
- ZSP540
- ZSP560
- ZSP600

Platform Features

- Low MCPs and Memory requirements
- Easy system integration
- Fully Compliance tested audio software suites
- Hardware Test and Development board available

Platform Benefits

- Easy-to-use and hassle-free system integration
- Scalable for future demands
- High-end audio and video quality



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VeriSilicon Solution Partners

The role of support hardware, software and services is critical in enabling customers to quickly and efficiently leverage DSP technology into their products. The success of DSP technology is reliant on a solid infrastructure that includes broad third-party support.

VeriSilicon has partnered with industry-leading technology providers to give you the ZSP technology support necessary to develop competitive products faster than ever and at lower cost than developing the technologies from scratch.

For audio applications, the following ZSP modules are now available:

- MPEG (MP3) Decoder
- WMA Decoder
- MPEG Encoder
- Ogg Vorbis Decoder
- MPEG AAC LC Decoder MPEG AAC LC Encoder
- SBC Decoder
- High Efficiency (aacPlus) Decoder
- SBC Encoder
- Dolby Digital (AC-3) Decoder
- FLAC Decoder
- Dolby Digital (AC-3) Consumer Encoder
- FLAC Decoder
- GSM AMR WB Decoder
- QSound MicroQ™
- SRS WOW HD™

For video applications, the following ZSP modules are now available:

- MPEG-4 Simple Profile Decoder
- H.264 Baseline Profile Decoder
- VC-1 (WMV9) Simple and Main Profile Decoder

Algorithm	ZSP410 MHz	ZSP210 MHz	Program ROM	Table ROM
MP3 decode	10.5 MHz	19.5 MHz	13.6 KW	10.9 KW
AAC decode	9.6 MHz	16.2 MHz	14.2 KW	9.7 KW
GSM AMR-NB	16.9 MHz	33.8 MHz	30.8 KW	31.6 KW

MHz is based on the worst case frame of the worst case test vector for that configuration.

H.264 Baseline Profile Decode	ZSP500 Resources
QCIF-15	14.2 MHz (1)
QVGA-30	82.4 MHz (2)
CIF-30	107.2 MHz (3)
Program Memory	29.6 KW
Data Memory	26 KW(4)

The in-loop deblocking filter is used for all performance numbers

- (1) Average MHz of Foreman QCIF test clip at 15 fps
- (2) Average MHz of Foreman QVGA test clip at 30 fps
- (3) Average MHz of Foreman CIF test clip at 30 fps
- (4) Additional memory for frame and bit stream buffers required



ZSP[®] Audio & Video Application Software



MPEG Decoder

- Decodes MPEG1 (ISO/IEC 11172-3) and MPEG2 (ISO/IEC 13818-3) audio bit streams.
- audio bit streams.
- Decodes non-ISO MPEG 2.5 low sample frequency (LSF) extension.
- Conforms to ISO/IEC 11172-4:1995 and ISO/IEC 13818-4:2004 standards.
- Layers I, II and III are all supported.
- Compile time customization options for reduced memory footprint:
 - Sixteen Bit Output
 - Layer I Enable/Disable
 - Layer II Enable/Disable
 - CRC Enable/Disable
- Includes mono, stereo, joint stereo, and dual channel modes

MPEG AAC LC Decoder

- MPEG AAC LC Decoder
- MPEG 2/4 AAC LC audio decoding [source, object] code software that complies with the following:
 - Decodes MPEG2 (ISO/IEC13818-7) & MPEG4 (ISO/IEC14496-3) audio bit streams.
 - Conforms to ISO/IEC 13818-4:1998/Amd 1:1999 and ISO/IEC 13818-4:2004 and ISO/IEC 14496-4:2000

High Efficiency (aacPlus) Decoder

- Decodes MPEG2 (ISO/IEC13818-7) & MPEG4 (ISO/IEC14496-3) audio bit streams.
- Conforms to ISO/IEC 13818-4:1998/Amd 1:1999 and ISO/IEC 13818-4:2004 and ISO/IEC 14496-4:2000
- aacPlus (HE-AAC) compliant (ISO/IEC 14496-3:2001/Amd.1:2003)
- Supported file types: adif, adts, and raw.
- Optimized for two channels: Mono, Stereo, or Dual Mono.

Dolby Digital (AC-3) Encoder

- Implements the Dolby Digital Consumer Encoder for reduced complexity
- Bitstream is fully compatible with ATSC Standard A/52A: Digital Audio Compression (AC-3) Standard, Rev. A
- Dolby Digital Consumer Encoder Test Vector Description, Version 3.2
- Designed with Dolby Digital Consumer Encoder Development Kit Version 2.2

MPEG Encoder

- Encodes MPEG1 (ISO/IEC 11172-3) audio bit streams.
- Bit streams are compliant with ISO/IEC 11172-4:1995(E) conformance standard.
- CBR, VBR, and free format support.
- Compile time customization options for reduced memory footprint:
 - Layer II Enable/Disable
 - Layer III Enable/Disable

MPEG AAC LC Encoder

- MPEG-2 AAC-LC and MPEG-4 AAC LC audio encoding ISO/IEC 13818 (Parts 1,2,3,7) and ISO/IEC 14496-3
- Constant, Absolute, and Variable Bit-rates
- Temporal Noise Shaping (TNS), Perceptual Noise Substitution (PNS), Mid/Side (M/S) Stereo
- ADIF (Audio Data Interchange Format) and ADTS (Audio Data Transport Stream)

Dolby Digital (AC-3) Decoder

- Compliant with:
 - Dolby Laboratories Multi-Channel Digital Audio Compression System.
- Test vectors provided in Dolby Digital Decoder Implementation Development Kit Version 3.0
- Meets ATSC Standard A/52A: Digital Audio Compression (AC-3) Standard, Rev. A
- Channels: 1 to 5.1 audio channels, compatible with Dolby Surround Sound.

WMA Decoder

- WMA decoder implementation that fully supports all versions of WMA, namely V2, V7, V8, V9, V9beta, V9NC, and VBR (Variable Bit Rate).
- Microsoft Quality Testing certified for WMA V2-V9 : 5kbps – 384 kbps

Ogg Vorbis Decoder

- An independent Ogg Vorbis I Decoder implementation based on the fully open, non-proprietary, patent-and-royalty-free Ogg Vorbis I specification from xiph.org.

SBC Decoder

- SBC decode for Low Complexity Subband Coding (SBC) bit streams defined in the Bluetooth Specification, Advanced Audio Distribution Profile (A2DP).

CORE FEATURES

- 16-bit signal controller (DSP/MCU)
- 16-bit MAC/32-bit ALU
- 1 inst./cycle with zero overhead looping
- Up to 220 MHz, 5-stage pipeline design
- Up to 220 million instructions/sec
- Available as synthesizable and FPGA netlists
- AMBA[™]/AHB support
- Fully static design
- JTAG debug interface



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GSM AMR Narrow-Band (NB) Decoder

- Decodes GSM AMR bit streams compliant with ETSI GSM 06.90.
- Includes Voice Activity Detection (VAD) ETSI GSM 06.93 and Discontinuous Transmission (DTX) ETSI GSM 06.94.

QSound MicroQ™

- Software digital audio engine enabling polyphonic ringtones, 3D game sound, and enhanced music play with multiple effects for mobile devices. Consists of the following [optional] components:
- mQsynth™ Polyphonic Wavetable Synthesizer
- mQ3DTM Positional 3D Audio Engine
- mQFXTM Digital Effects
 - QXpander®
 - QSizzle™
 - QRumble™
 - QVerb™
 - QCompressor™
 - QEqualizer™
 - QLimiter™
 - QLoudness™
- QXpander® 3D Spatial Processing

SRS WOW HD™

- Total audio enhancement solution developed by industry's leading consumer audio experts at SRS Labs
- Designed to deliver the best sound experience for stereo playback devices that includes eight key features
 - SRS®, SRS Headphone™, SRS FOCUS™, SRS Mono 3D™, SRS TruBass®
 - Center Control, Limiter, Definition™

SRS TruSurround HD™

- Leading-edge multichannel virtualization technology
- Ideally suited for midrange and high-end television
- Utilizes SRS Labs proprietary algorithms for optimal bass performance, dialog clarity, maximum high-frequency clarity

GSM AMR Wide-Band (WB) Decoder

- Decode the Extended Adaptive MultiRate Wideband bitstreams compliant with 3GPP TS 26.290: "Audio codec processing functions; Extended Adaptive Multi-Rate – Wideband (AMR-WB+) codec; Transcoding functions".
- Compliant with 3GPP TS 26.274: "Speech codec speech processing functions; Extended Adaptive Multi-Rate – Wideband (AMR-WB+) speech codec; Conformance testing".

MPEG-4 Simple Profile Decoder

- ISO/IEC 14496-2/4
- Fully Compliance tested (ISO/IEC 14496-4)
- Level 0,1,2,3 support
- H.263 baseline profile decoding
- Elementary bitstream input
- Output in YUV 4:2:0 format
- Integrated adaptive de-blocking filter (optional post processing block)

VC-1 (WMV9) Simple/Main Profile Decoder

- SMPTE 421M-2006 Television
- Fully Compliance tested (SMPTE RP228)
- Simple Profile - Low and Medium level
- Main Profile - Low, Medium and High level
- Elementary bitstream input
- Output in YUV 4:2:0 format
- Integrated adaptive de-blocking filter (in-loop)

H.264 Baseline Profile Decoder

- ISO/IEC 14496-10 (MPEG4 AVC)
- Fully Compliance tested
- Baseline Profile up to level 3
- Elementary bitstream input
- Output in YUV 4:2:0 format
- Integrated adaptive de-blocking filter

About VeriSilicon

VeriSilicon Holdings Co., Ltd ("VeriSilicon") is a fast growing silicon solutions company providing products and services that enable customers to meet their chip design objectives, accelerate development programs and deliver market proven silicon products - on time and at lower cost. VeriSilicon specializes in providing expert design services, market leading ZSP® licensable cores and platforms, industry standard semiconductor IP and scalable ASIC turnkey services across a broad range of application markets, including multimedia, voice and wireless communications. VeriSilicon has design, operation and sales and support offices in Santa Clara, California, Dallas, Texas, Shanghai and Beijing, China, Taipei, Taiwan, Tokyo, Japan, Nice, France and Seoul, Korea. For more information, visit www.verisilicon.com.

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