

ZSP[®]600 Quad-MAC Superscalar Core



OVERVIEW

The ZSP600 is a quad-MAC superscalar DSP core that addresses the high performance data throughput and signal processing requirements of emerging communications platforms. As the first released core in VeriSilicon's second generation ZSP family, the ZSP600 provides an optimized solution for MAC intensive communication algorithms. The ZSP600 supports up to six IPC (instruction/cycle) DSP performance at a peak 300MHz data rate. It includes quad-MAC and quad-ALU computational resources, high-performance load/store memory architecture, and dedicated co-processor interfaces, combined with state-of-the-art power reduction techniques. These attributes make the ZSP600 core an ideal solution for a variety of embedded DSP algorithms, including those required for wireless infrastructure, mobile (3G), IAD/home gateway, central office, and access/network applications.

From a programming perspective, the ZSP600 is successor architecture to the ZSP400 that supports backward compatibility at the assembly level, facilitating reuse of ZSP400 code. ZSP600 instruction parallelism is supported by user-transparent instruction grouping and pipeline control to deliver superscalar DSP performance, while programming using a RISC-instruction set. The ZSP600 is supported by a choice of C-based programming environments and a complete tool chain, including system level and co-verification support. A broad range of highly-optimized algorithms is available from leading third party software developers in the VeriSilicon Solution Partners Program, and is supported by VeriSilicon's ZOpen[™] Software Framework.

FEATURES

- Six-issue superscalar architecture
- Complete C-based software tool chain
- Four Multiplier-Accumulators
- Four ALUs (Two 40-bit and two 16-bit)
- Eight instruction/cycle pre-fetch
- Dual 64-bit data interfaces with dedicated addressing
- Enhanced register file and large address space
- Orthogonal instruction set
- Synthesizable RTL and hard macro versions available
- 300MHz peak operation, fully static design
- Reduced power modes of operation
- Dual ACS – Viterbi (add-compare-select) per cycle
- JTAG interface with optional embedded trace/debugger/profiling
- Bi-directional co-processor/hardware acceleration interface

BENEFITS

- High-performance RISC-based programming
- Outstanding code density/efficiency using C-compiler
- Suitable for wide range of communication algorithms
- Optimized for low power applications
- Synthesizable RTL for migration and flexibility
- Embedded real-time trace

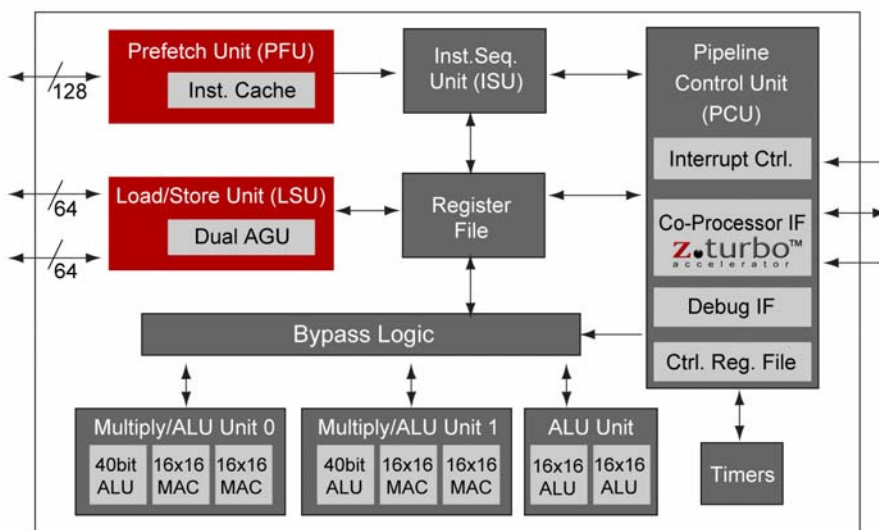


Figure.1 Simplified ZSP600 Block Diagram



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DESCRIPTION

The ZSP600 is a fully synthesizable, single-phase, clocked architecture, with all core I/Os registered for ease-of-process migration and design flexibility. The ZSP600 is available as a licensable DSP IP core.

The ZSP600 provides extensive computational resources, including four 16-bit multipliers/MACs, dual 40-bit ALUs, and dual 16-bit ALUs, all capable of supporting 16-and 32-bit operations. The ZSP600 can perform four independent 16×16 MUL/MAC operations into four 16-bit or two 40-bit results, two 32×32-bit MUL/MACs into a 32-bit result, or two Viterbi (add-compare-select) results per cycle.

The ZSP600 is based upon a high-bandwidth memory architecture with separate 8 instruction per cycle per fetch and dual 64-bit data interfaces (supporting Harvard architecture), over a 24-bit address space. The instruction memory architecture allows multi-instruction/cycle pre-fetch (up to 8 words per cycle) to an integrated instruction cache. The data memory architecture incorporates dual independent 64-bit load/store units, with dedicated address generation, allowing up to eight 16-bit word or four 32-bit word load/store operations per cycle. The ZSP600 integrates a bi-directional co-processor interface to support hardware acceleration. The memory subsystem (MSS) is decoupled from the DSP operations to provide increased flexibility in support of different memory schemes. In addition, optional AMBA™/AHB interfaces for simplified on-chip system integration are available. ZSP600 integration is available for optional on-chip embedded trace/profiling module blocks that interface with JTAG-based hardware-assisted debugger support (for heterogeneous and homogenous multi-processor systems).

The ZSP600 is instruction set compatible with the ZSP400 core, supporting assembly code and ZSP400 legacy applications code reuse and simplified design migration. It also includes instruction set enhancements to ZSP400 RISC architecture for improved broadband and wireless application support.

About VeriSilicon

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