

ZSP[®]500 – Power Optimized Superscalar DSP Core



OVERVIEW

The ZSP500 represents the best price/performance solution for a DSP core in its class for next generation mobile communications and multimedia-rich consumer applications. The ZSP500 is a superscalar DSP architecture; enabling execution of up to four instructions, including two multiply accumulates (MACS) per clock cycle. Operating at up to a 400 MHz clock rate, the ZSP500 can achieve 1600MIPS of peak processing power and 800 million sustained MACs/second. The ZSP500 core features scalable performance, an extensible instruction set, a configurable memory, co-processor port and SoC-ready platform interfaces.

Optimized to achieve the right price/performance ratio needed for programmable broadband platforms, the ZSP500 processor features many enhancements for programmability, code density, and performance for arithmetic-intensive algorithms. The ZSP500 also features advanced power management, both automatic (transparent to the programmer) and software programmable, to provide a power efficient implementation for mobile applications. Debugging and embedded real-time trace capabilities, unrivalled in any licensable DSP, provide optimal capabilities for rapid debugging of integrated hardware and software solutions. An external Memory Sub-System (MSS) can be configured to support either Harvard or unified memory maps and provides industry standard interfaces (AMBA[™]/AHB) for simple integration to SoC platforms.

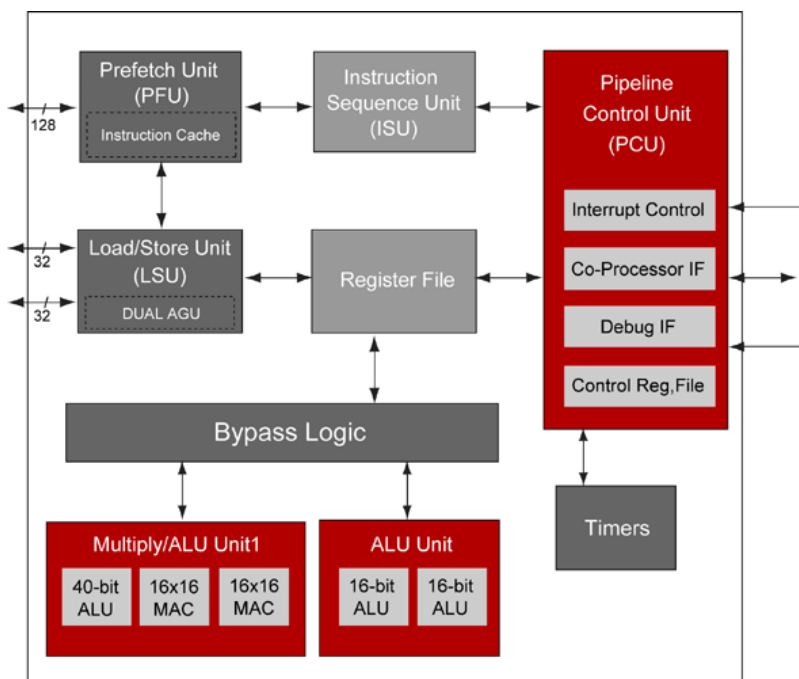


Figure 1. Simplified ZSP500 Block Diagram

FEATURES

- 400MHz operation, fully static, 8-stage pipeline design
- Four-issue superscalar architecture
- Choice of integrated software tool chains
- Dual Multiplier-Accumulators
- Tree ALUs (One 40-bit and two 16-bit)
- Orthogonal instruction set
- Dual 32-bit data interfaces with dedicated address generation
- configurable memory space
- 24-bits instruction/data address range
- Synthesizable RTL and hard macro version available
- Automatic and software controlled power management
- JTAC debug interface
- Optional real time trace
- Bi-directional co-processor/hardware acceleration interface

BENEFITS

- High-performance RISC-based programming
- Outstanding code density/efficiency using both C-compiler and assembler
- Suitable for wide range of consumer and communication algorithms
- Optimized for low power applications
- Synthesizable RTL for migration and flexibility
- Real time hardware debugging



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The ZSP500 implements the ZSP[®] G2 (second generation) instruction set, providing software compatibility with the ZSP400 (first generation) core and the ZSP600 (also a G2 core), enabling code reuse and effortless design migration. The ZSP500 instruction parallelism is supported by user transparent instruction grouping and pipeline control, which eliminates programming hazards common to most high performance DSP architectures. The ZSP500 also features instruction set extensibility, utilizing an advanced bi-directional co-processor interface for adding new custom instructions with logic acceleration. The ZSP500's Software Development Kit (SDK) code profiling tools identify hot spots for instruction set optimization.

The ZSP500 is supported by two C-language based integrated development environments that feature an optimizing C-compiler, assembler, linker, debugger, cycle-accurate simulators, project management, and a host of other features. Extensive sets of hardware and software tools are available that extend this support environment to include: multi-core debugging, trace, architecture validation, synthesis, behavioral modeling, simulation, profiling, emulation, co-verification, SoC integration, task management, and scheduling (RTOS). The ZSP500 is supported by an open application software framework (ZOpen[™]), which can rapidly integrate production-quality software modules that are available off-the-shelf from VeriSilicon Solution Partners.

An AMBA[™]/AHB interface is provided for simplified on-chip integration. This provides for a seamless interface to platform level IP implementations integrating multiple ZSP500's, a host RISC microprocessor and peripherals. This hardware level interface is further enhanced by ZOpen[™] based software drivers, APIs and host control software functions to rapidly bring up RISC + DSP application programs.

The ability of the SoC developers to achieve fastest time-to-market with ZSP500 core-based designs is further enhanced by the most comprehensive on-chip embedded trace/profiling module blocks in the licensable DSP industry. The configurable debugging blocks interface with JTAG-based hardware assisted debugger support (for heterogeneous or homogeneous multi-processor systems). The on-chip Embedded Trace Module (ETM) capabilities provide for the triggering of real time trace data, based on a highly flexible combination of program and data value and/or address values. These ETM and debugging blocks can be configured out of the system when targeting volume production requirements.

About VeriSilicon

VeriSilicon Holdings Co., Ltd ("VeriSilicon") is a fast growing silicon solutions company providing products and services that enable customers to meet their chip design objectives, accelerate development programs and deliver market proven silicon products - on time and at lower cost. VeriSilicon specializes in providing expert design services, market leading ZSP[®] licensable cores and platforms, industry standard semiconductor IP and scalable ASIC turnkey services across a broad range of application markets, including multimedia, voice and wireless communications. VeriSilicon has design, operation and sales and support offices in Santa Clara, California, Dallas, Texas, Shanghai and Beijing, China, Taipei, Taiwan, Tokyo, Japan, Nice, France and Seoul, Korea. For more information, visit www.verisilicon.com.

For more information please contact:

• US

VeriSilicon, Inc.
4699 Old Ironsides Dr., Suite 350
Santa Clara, CA 95054
Tel: +1 408 844 8560
Fax: +1 408 844 8563
E-mail: us-sales@verisilicon.com

VeriSilicon, Inc.

500North Central Expressway
Suite 430 Plano, Texas 75074
Tel: +1 972 244 5100
Fax: +1 972 244 5101
E-mail: us-sales@verisilicon.com

• China

VeriSilicon Microelectronics (Shanghai) Co., Ltd.
Building 1, No.200, Zhangheng Rd
Pudong New Area, Shanghai 201204
Tel: +86 21 51311118
Fax: +86 21 51311119

VeriSilicon Microelectronics (Beijing) Co., Ltd.

Rm A106, Information Center,
Zhongguancun Software Park
8 Dongbeiwang West Road,
Haidian District, Beijing 100193, P.R.C
Tel: +86 10 8282 5201
Fax: +86 10 8282 5201
E-mail: china-sales@verisilicon.com

• Taiwan

VeriSilicon Taiwan, Inc.
5F, No. 306, Sec.1., Neihu Road
Taipei 114, Wall Street Building, Taiwan.
Tel: +886 2 2656 2606
Fax: +886 2 2656 2604
E-mail: taiwan-sales@verisilicon.com

• Japan

VeriSilicon K.K.
The Imperial Tower, 8th floor
1-1-1 Uchisaiwaicho Chiyoda-ku
Tokyo, 100-0011 Japan
Tel: +81 3 3507 3005
Fax: +81 3 3507 3006
E-mail: japan-sales@verisilicon.com

• Europe

VeriSilicon, SARL
Les Algorithmes, Bat. Aristote A 2000 Route
des Lucioles 06901 Sophia Antipolis, France
Tel: +33 4 9294 4892
Fax: +33 4 9294 4882
E-mail: europe-sales@verisilicon.com

• Korea

VeriSilicon, Korea.
B-1201, The O superium 1, 3001-2,
Bangbae 4-dong, Seocho-gu Seoul, 137-064, Korea
Tel: +82 2 6409 4506
Fax: +82 2 6409 4501
E-mail: korea-sales@verisilicon.com

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