

ZSP[®]200 Very Low Power Compact DSP Core



OVERVIEW

The ZSP200 DSP core fills the processing gap between licensable microprocessors and higher-end DSPs, making it ideally suited for high volume applications such as disk-drive controls, industrial controls, toys, electronic games, VoIP terminals and security devices. Based on the widely-adopted first generation (G1) ZSP architecture, the ZSP200 core utilizes proven technology and is fully supported by development and EDA tools, and applications software, enabling shortest time-to-market at very low risk. Development time and effort are especially reduced by the ZSP200's intrinsic ability to allocate its processing resources automatically without burdening the programmer with data and resource dependencies and hazards. This improves compiler efficiency and greatly reduces the need for time consuming "hand crafting" of code, unlike traditional DSP and VLIW architectures.

With careful attention to core compactness and power management, the ZSP200 core has been specifically targeted to offer optimized performance with very low energy consumption and low cost. It therefore represents an ideal replacement to existing RISC-based SoC, that may be either struggling to support processing requirements, or consuming too much power.

The ZSP200 core is a 16-bit, fixed-point superscalar DSP that utilizes a Harvard architecture to maximize program and data concurrent memory fetches/instruction execution. With two processing units and a five-stage pipeline, the ZSP200 is capable of sustaining 300 MIPS peak performance when clocked at 150MHz. The ZSP200's comprehensive, orthogonal instruction set utilizes 16-bit instructions and single-cycle instruction execution to help you achieve high throughput, small footprint code with minimal effort. The hardware-controlled pipeline makes the ZSP200 core much easier to program and debug than typical DSP architectures, and its 2-issue instruction feed ensures efficient use of the ZSP200's processing units at all times. The ZSP200 is available with interfaces to the popular AMBA bus architecture and is well suited for rapid development SoC projects.

FEATURES

- Dual-issue superscalar architecture, providing up to 300MIPS performance in 0.18 μ m
- 16-bit multiplier-accumulator with 32-bit multiplication support
- Dual 16-bit ALUs with single-cycle 32-bit operation support
- Two 40-bit accumulators
- Add-compare-select instructions for Viterbi acceleration
- Simple, orthogonal, 16-bit instruction set
- Binary compatible with ZSP400
- Complete integrated development environment for Windows, Solaris and Linux
- Wide range of application software available
- Synthesizable RTL and hard macro versions available
- Automatic and software controlled power management functions
- IEEE1149.1 compliant JTAG interface for debug and test
- Worldwide network of solutions engineers

BENEFITS

- High performance for control and signal processing
- Unrivalled 32-bit performance for low cost DSP
- Low-risk, rapid development of software applications
- Small footprint solutions with very compact code
- Easy migration to higher performance ZSP cores
- World-leading technical support



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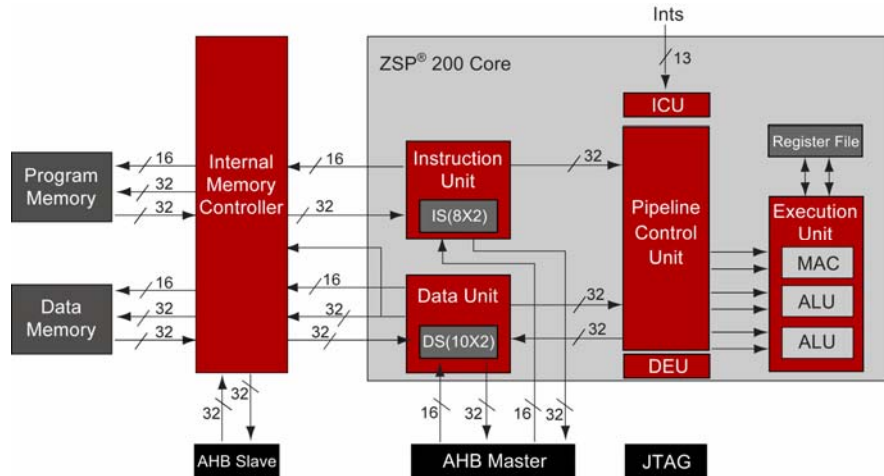


Figure 1. ZSP200 Digital Signal Processor for System-on-a-Chip (SoC)

ZSP200 implements the ZSP G1 instruction set, providing binary compatibility with the ZSP400 core and forward compatibility with all ZSP G2 cores (ZSP500 and ZSP600) enabling code reuse and easy design migration. The ZSP200 instruction parallelism is supported by instruction grouping and pipeline control that are transparent to the user, eliminating programming hazards common to most high performance DSP architectures. The ZSP200 is supported by the ZSP Software Development Kit (SDK), which provides code profiling tools to identify hot spots for instruction set optimization. The ZSP200 is supported by two C-language based integrated development environments (from Green Hills Software) that feature an optimizing C-compiler, assembler, linker, debugger, simulators, project management and a host of other features. Extensive sets of hardware and software tools are available that extend this support environment to include: cross assembly, multi-core debugging, trace, architecture validation, synthesis, behavioral modeling, simulation, profiling, emulation, co-verification, SoC integration, task management and scheduling (RTOS).

The ZSP200 is compatible with the ZSP Open Application Software Framework (ZOpen™), which can rapidly integrate production-quality software modules that are available off the shelf from VeriSilicon Solution Partners. The provisions of software drivers, APIs and host control software further enhance this hardware level interface and enable you to rapidly bring up RISC/DSP applications. An AMBA/AHB interface is provided with a complete example system, synthesis and timing analysis scripts and detailed implementation information for simplified on-chip integration. This provides for a seamless interface to platform level IP implementations integrating a ZSP200 and a host RISC microprocessor. The ZSP200 is available in soft (RTL) form for maximum flexibility, or as a hard macro for lower cost and simpler integration.

About VeriSilicon

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