

# VSI403WLP Digital Signal Processor

## Wafer Level Package



### OVERVIEW

The VSI403WLP is an extremely low power 16-bit fixed-point digital signal processor (DSP) based on the VeriSilicon ZSP400 DSP core, running less than 250 $\mu$ W per DSP MIPS (MMAC). The device is packed at a wafer level to create a bumped die product that can be mounted directly on a multi-chip module or printed circuit board with same reliability and performance characteristics as packaged ICs. VSI403WLP is designed for consumer handheld applications such as VoWiFi and Audio. The VSI403WLP is capable of a maximum clock rate of 150 MHz for 600 MIPS peak performance and sustained effective throughput of 300 DSP MIPS (MMACs). The device is also software compatible with all other products in the ZSP architecture, and offers an unrivalled combination of code density, performance and ease of use.

### MEMORY

The internal memory structure of the VSI403WLP comprises of 16K words of instruction memory, 16K words of data memory, 16K words of configurable memory for instruction or data, 1K words of memory for boot loading and interrupt support and peripherals. Additionally, the external memory interface unit interfaces the VSI403WLP to external memory devices. Both asynchronous and synchronous devices are supported. The external memory is logically segmented into instruction, data, and peripheral spaces.

### DMA

The DMA controller of the VSI403WLP supports zero-over-head instruction or data transfers to or from the entire 48K words of internal RAM to the memory interface unit, host processor interface, or a serial port. The eight DMA channels are segmented between four "indexed" and four "non-indexed" channels. Indexed channels have the ability to buffer data from either of the serial TDM interfaces, and non-indexed channels perform sequential accesses to or from internal memory. All DMA channels feature an auto-reload capability to restart transfers with no processor overhead.

### Features

- 150 MHz operation at 1.2V
- 2 high-speed serial/TDM ports (T1/E1 framer, H.100/H.1 10 bit stream compatible)
- Low power dissipation (50mW typical at 150 MHz)
- Sleep power mode consumes <20 $\mu$ W/MHz
- 48K words on-chip RAM
- 8-channel DMA controller
- On-board PLL for clock generation
- 32-/16-bit external memory interface
- 2 on-board timers
- 8-bit host processor interface with hardware byte pack/unpack
- IEEE 1149.1-compliant JTAG port for in-system debug

### Benefits

- Ideal for low-cost VoIP designs
- Direct interfacing to standard telecommunications interfaces, reducing system cost
- Low power per voice or audio channel
- Suitable for very low power applications
- High data throughput without processor overhead
- Flexibility to optimize power consumption
- High data bandwidth to off-chip devices
- Simple interfacing to industry-standard micros
- Low overhead on chip debug

Figure 1. VSI403WLP Functional Block Diagram



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### TIMERS

The VSI403WLP has two identical 16-bit on board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit prescaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

### TDM SERIAL PORTS

The VSI403WLP provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers, which can be either burst or continuous, with a maximum clock speed of one-half the processor clock. Both serial ports support  $\mu$ - and A-law hardware companding and provide the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/H.1 10 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.

### HOST PROCESSOR INTERFACE (HPI)

The Host Processor Interface, or HPI, is an asynchronous 8-bit parallel port that is used to interface with off-chip devices. It is compatible with both Motorola and Intel style memory interfaces, and supports word transfers. The maximum transfer rate for the HPI is one-third of the processor clock frequency. The HPI includes hardware support to pack/unpack bytes to/from 16-bit words, removing the overhead of this task from the ZSP400 core.

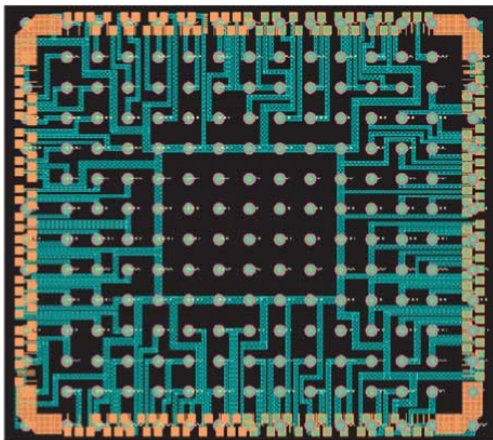


Figure 2. VSI403WLP Bump Pattern Layout

### About VeriSilicon

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