VSI403LC
Digital Signal Processor

ZSP® PERFORMANCE AT ULTRA-LOW COST WITH VERY LOW POWER CONSUMPTION

The VSI403LC is an extremely low-cost and low-power 16-bit fixed-point digital signal processor (DSP) based on the VeriSilicon's ZSP®400 DSP core, running less than 200µW per DSP MIPS (MMAC). The device has been designed for applications requiring high throughput and flexibility coupled with a high speed I/O, such as Voice over Packet CPE devices and consumer audio applications. The VSI403LC is capable of a maximum clock rate of 120 MHz for 480 MIPS peak performance and sustained effective throughput of 240 DSP MIPS (MMACs). The device is also software compatible with all other products in the ZSP architecture, and offers an unrivalled combination of code density, performance and ease of use.

MEMORY

The internal memory structure of the VSI403LC comprises of 16K words of instruction memory, 16K words of data memory, 16K words of configurable memory for instruction or data, 1K words of memory for boot loading and interrupt support and peripherals. Its large on-chip memory eliminates the need for external memory which dramatically reduces system power associated with accessing high-speed SRAM.

DMA

The DMA controller of the VSI403LC supports zero-overhead instruction or data transfers to or from the entire 48K words of internal RAM to the memory interface unit, host processor interface, or a serial port. The eight DMA channels are segmented between four "indexed" and four "non-indexed" channels. Indexed channels have the ability to buffer data from the serial TDM interface, and non-indexed channels perform sequential accesses to or from internal memory. All DMA channels feature an auto-reload capability to restart transfers with no processor overhead.

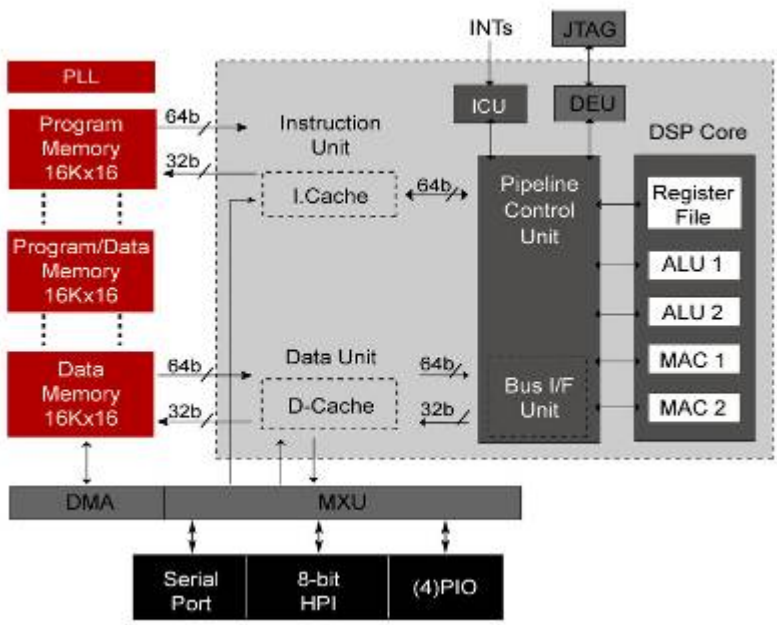

Figure 1. VSI403LC Functional Block Diagram

Applications:

- Evaluation of ZSP400 DSP core
- Development of software for ZSP400 and VSI403LP
- DSP algorithm benchmarking
- Rapid-prototyping of DSP-based products
- System integration with other hardware

Features

- VSI403LP Evaluation Board (EB403)
- Full-featured, ZSP Software Development Kit (SDK)
- 30-Day Evaluation of GHS MULTI Tools
- EB403 Board Support Package
- Tutorials
- Example Source Code
- MP3 and MASC Codec Demonstrations
- Comprehensive Documentation

Benefits

- All-in-one bundled kit for efficient development
- Value-priced below cost of competitive software tools
- Quick evaluation of ZSP400 core / VSI403LP device
- Enables development before customer hardware available
- Accelerates time-to-market

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TIMERS

The VSI403LC has two identical 16-bit on board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit prescaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

TDM SERIAL PORT

The VSI403LC provides a synchronous serial port that supports 8 or 16-bit active or passive transfers, which can be either burst or continuous, with a maximum clock speed of one-half the processor clock. The serial port supports µ- and A-law hardware companding and provides the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.

HOST PROCESSOR INTERFACE (HPI)

The Host Processor Interface, or HPI, is an asynchronous 8-bit parallel port that is used to interface with off-chip devices. It is compatible with both Motorola and Intel style memory interfaces, and supports word transfers. The maximum transfer rate for the HPI is one-third of the processor clock frequency. The HPI includes hardware support to pack/unpack bytes to/from 16-bit words, removing the overhead of this task from the ZSP400 core.

DEVELOPMENT TOOLS

The VSI403LC is fully supported by both VeriSilicon and 3rd party commercial tools, including the VSI GNU-base SDK and the Green Hills Software MULTI® software development tools. The ZSP architecture enables the C compilers to produce code unrivaled in code density and execution speed by any DSP in its class, offering fast time to market with optimal performance and cost.

VeriSilicon offers a complete integrated development kit called the DK403. The DK403 integrates a high-performance DSP evaluation board, USB JTAG controller, full-version software development tools, a board support package, example source code, tutorials and complete documentation, making it the most comprehensive DSP development kit available in the industry today.

About ZSP Reference Silicon:

ZSP Reference Silicon is VeriSilicon's range of voice processors based on the ZSP400 DSP core, which support board-level voice products and enable quick prototyping of voice SoCs. These processors are ideal for VoIP customer premises equipment (CPE) for residential, SOHO and enterprise applications. They are also targeted for other voice-related applications such as compression, recognition, noise reduction and echo cancellation. For more information, please visit http://www.verisilicon.com/Products & Solutions

About VeriSilicon

VeriSilicon Holdings Co., Ltd ("VeriSilicon") is a fast growing silicon solutions company providing products and services that enable customers to meet their chip design objectives, accelerate development programs and deliver market proven silicon products - on time and at lower cost. VeriSilicon specializes in providing expert design services, market leading ZSP® licensable cores and platforms, industry standard semiconductor IP and scalable ASIC turnkey services across a broad range of application markets, including multimedia, voice and wireless communications. VeriSilicon has design, operation and sales and support offices in Santa Clara, California, Dallas, Texas, Shanghai and Beijing, China, Taipei, Taiwan, Tokyo, Japan, Nice, France and Seoul, Korea. For more information, visit www.verisilicon.com.

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