ZSP® in Voice Over Data Network Applications White Paper

Trademark Acknowledgments

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1. Designed for Voice Over Data Network Application

Voice over Network (VoN) technology is one of the fastest growing areas of telecommunications. The initial impetus was cost reduction for intra-company long distance phone calls. By integrating voice traffic into the data network they utilized excess bandwidth and removed the overhead of maintaining a voice only network. They quickly realized a very significant cost reduction. Now the technology is rapidly expanding into the consumer market, and as it grows the underlying infrastructure is in place to offer more sophisticated interaction of voice and data services. The ZSP architecture is ideally suited for voice over network applications, offering a superior combination of performance, efficient memory usage, and ease of use at a very competitive price.

VoN applications include:

- IPBX
- Voice over DSL
- SOHO gateways
- Access concentrators
- Routers

2. DSP Requirements of Voice Over Networks (VoN)

Voice over Networks utilize a number of technologies, including Internet Protocol (IP), Asynchronous Transfer Mode (ATM), Frame Relay (FR), and Digital Subscriber Line (DSL). The voice traffic is introduced into an IP network in a number of ways: direct with an IP phone, via CTI-style gateways supporting multiple analog telephone lines, via gateways between legacy PBX systems and the IP network, and via routers or PBXs with integrated gateway functionality.

DSP technology is at the core of this voice and data network integration, enabling the echo cancellation and voice compression needed so voice traffic can efficiently ride over packet networks while maintaining acceptable voice quality. This technology is integral to all voice over data network systems and consists of both the hardware and software needed to implement standard DSP algorithms in a real-time packet network application.

Three of the most important factors in choosing a DSP for voice over network applications are performance, cost per channel and time to market.

3. Performance

Among the most severe degrading factors of VoN voice quality are echo and network delay. Echo can be introduced both by impedance mismatches in the network and by acoustic coupling between speaker and microphone at the far-end terminal. Delay—which is introduced by encoding, propagation, buffering, and decoding—worsens the effect of echo in the VoIP system. Thus, echo cancellation must be implemented in order to offer good quality voice service.

The International Telecommunications Union (ITU) has defined performance requirements for echo cancellers in its G.165 specification, soon to be replaced by the more stringent G.168 version. These specifications leave plenty of scope for voice over network product developers to enhance, and thereby differentiate, their products. Tailoring the echo tail length to exactly meet differing requirements enables cost reduction to be finely tuned, emphasizing the importance of using a programmable DSP.

The ease of use of ZSP processors offers the fastest turnaround of these system optimizations while letting you achieve market-leading channel densities.

4. Cost Per Channel

Maintaining a low cost per channel is a major factor in VoN applications. This means the DSP must be capable of supporting a large number of channels relative to board area and power consumption. Although the underlying algorithms within each market segment of voice over networks are the same, each product places different demands on the system designer to achieve the lowest cost per channel. Currently, standard DSP products are generally used, with the possible exception being IP telephones. As cost continues to be driven down, product needs will split between high performance processor devices for routers and integrated DSP/microprocessor/peripheral devices for Customer Premises Equipment (CPE) and PBXs.

Only the ZSP architecture has partners who offer the system-on-a-chip expertise and IP portfolio that will meet these market requirements in the short, medium, and long term.

5. Time-to-Market

Bringing a product out quickly, along with the need for flexibility in load sharing, demands a DSP with a C-compiler that can produce compact and efficient code without needing handcrafted assembly language. Recent VLIW architectures offer compilers that do not produce very compact code, and the wide memories required contribute significantly to high power consumption. Conventional DSP architectures that have been enhanced to include dual multipliers and other extensions offer high channel density. However, their non-orthogonal instruction sets can require assembly language programming to achieve full potential.

The RISC-like, super-scalar ZSP architecture provides a far better alternative, offering the channel densities required with less programming effort and more

efficient memory use. Current processors based on this architecture, such as the VSI401Z and VSI402ZX from VeriSilicon are capable of implementing more than twice the number of channels compared to any other single processor core device with comparable memory usage.

6. Summary

The voice over networks market is rapidly expanding, and as it does is becoming increasingly competitive. In order to be successful in this market, it's important to offer a high performance product at a low cost. To achieve this means having a flexible yet powerful programmable DSP architecture with a roadmap to higher levels of performance and rapidly decreasing cost per channel.

Only the ZSP architecture offers a viable roadmap to meet all the demands of this market with silicon that is available for design today.