

ZSP[®]neo

Ultra Compact Signal Controller Core



OVERVIEW

The ZSPneo signal processor controller core is a highly optimized core that focuses on cost and power consumption. It is a ZSP[®] G1 architecture implementation that can deliver up to 150 MIPS on a 0.18 process and up to 220 MIPS on a 0.13 process. The core includes a single-cycle multiply-accumulate unit to deliver good DSP performance along with efficient control capabilities.

TARGET APPLICATIONS

- Embedded Control
- Toys (speech synthesis and animation control)
- Sound synthesis
- MP3 playback
- Voice over IP
- Servo control

BENEFITS

- High performance upgrade for 8/16-bit controllers
- DSP performance without overhead of 32-bit instructions
- Single core for system control and signal processing
- Ultra low power consumption
- Very small footprint for low-cost deployment in silicon

CORE FEATURES

- 16-bit signal controller (DSP/MCU)
- 16-bit MAC/32-bit ALU
- 1 inst./cycle with zero overhead looping
- Up to 220 MHz, 5-stage pipeline design
- Up to 220 million instructions/sec
- Available as synthesizable and FPGA netlists
- AMBA[™]/AHB support
- Fully static design
- JTAG debug interface

ARCHITECTURE FEATURES

- Embedded control processing efficiency
- Compact 16-bit standard instruction set
- Extensive 32-bit operand support
- Easy to program, orthogonal instruction set
- Load/store based instruction set
- Outstanding code density

SUPPORT

- Highly optimized C-Compilers
- Local support by ZSPneo authorized partners around the world

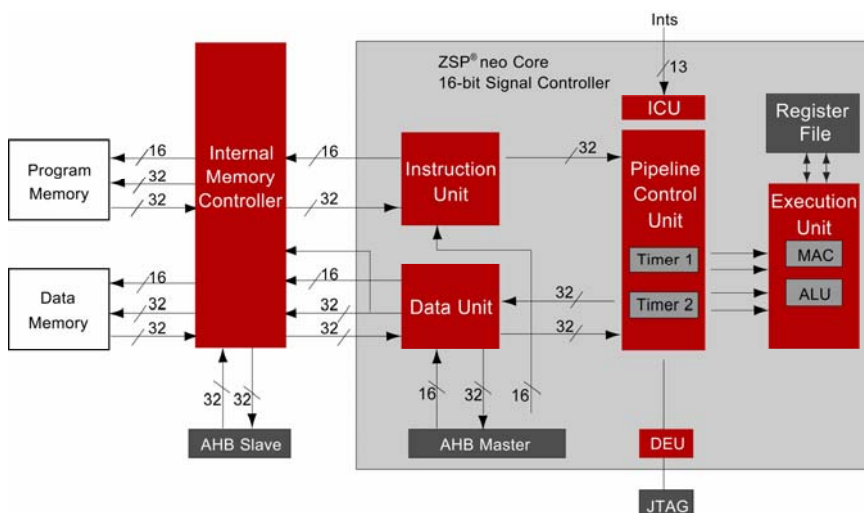


Figure 1. ZSPneo Signal Controller Core



ZSP[®]neo Ultra Compact Signal Controller Core

ZSPneo-ULTRA COMPACT SIGNAL CONTROLLER CORE

ZSPneo core is available in a generic technology (gtech) and FPGA netlist forms allowing licensees to retarget to desired library and process technology. ZSPneo is binary compatible with the ZSP200 and ZSP400 cores allowing users of the core to seamlessly scale to a higher digital signal processing capabilities using the exact same software base.

SoC INTEGRATION SUPPORT

- AMBA[™]/AHB (optional) or native ZSP bus interfaces are available
- Co-verification and System modeling support available

AVAILABLE ZSPneo SOFTWARE DEVELOPMENT SOLUTIONS

- Highly optimized development kits available
- JTAG probes for single/multi-core support available
- ZOpen[™] Software Development Framework enables rapid integration and reuse of software modules developed different 3rd parties

AVAILABLE ZSPneo HARDWARE DEVELOPMENT SOLUTIONS

- Architecture evaluation boards
- Standalone FPGA prototyping boards

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